DRS U6000 640x480 VO_X Uncooled IR Focal Plane

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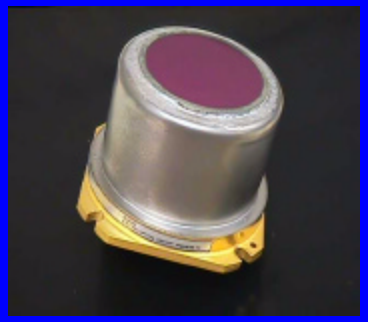
Topic Outline

- DRS VO_X uncooled focal plane product technology
- Small pixel size advantages
- U6000 640x480 product objectives
- U6000 product capabilities
- Design validation
- Video
- Summary

The U3000 320x240 Product

IMAGER MODULE

RADIAMETER MODULE



- *51 ㎛ pixel size*
- *320x240 array format*
- *TV compatible at 60 frames/Sec*
- *Vacuum packaged with thermal electric cooler, temperature sensor, refirable vacuum getter*
  - *Imager*
  - *Radiometer – with internal stray thermal radiation shield*
- *Thousands delivered to customers worldwide*

DRS TECHNOLOGIES

The U4000 320x240 Product

- 2-Fold NETD performance improvement
- External programming of key on-chip functions using “Smart-Sensor” parallel 6-bit data interface between sensor and UFPA
  - 6-bit pixel offset compensation for higher signal gain and improved spatial pattern noise
  - Signal gain selection over > 6:1 range
  - On-chip 6-bit resolution detector bias selection with 100:1 external bias drift rejection
- Precision UFPA temperature measurement streamed onto video line during blanking

DRS 320x240 UFPA INTEGRATED WITH CAMERA ELECTRONICS (NYTECH)

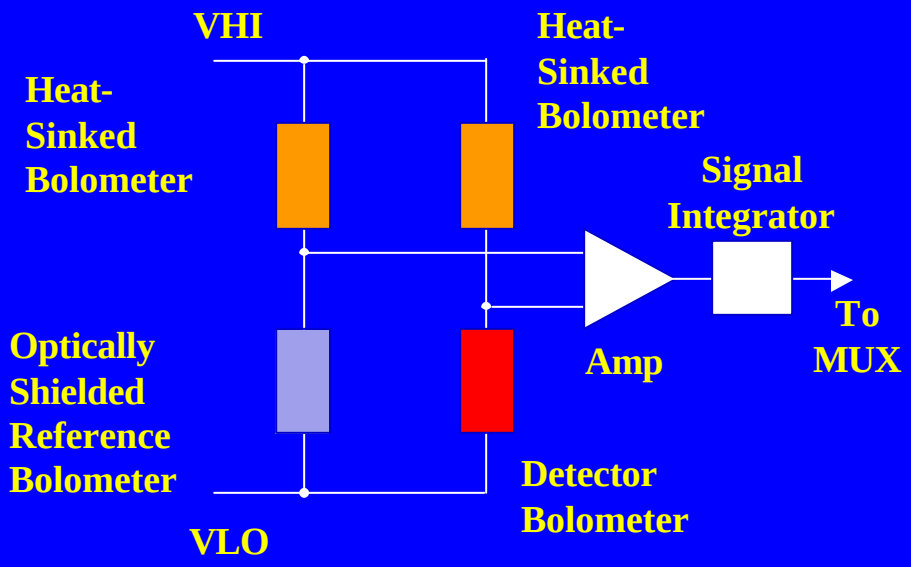
Small Pixel Size Advantages

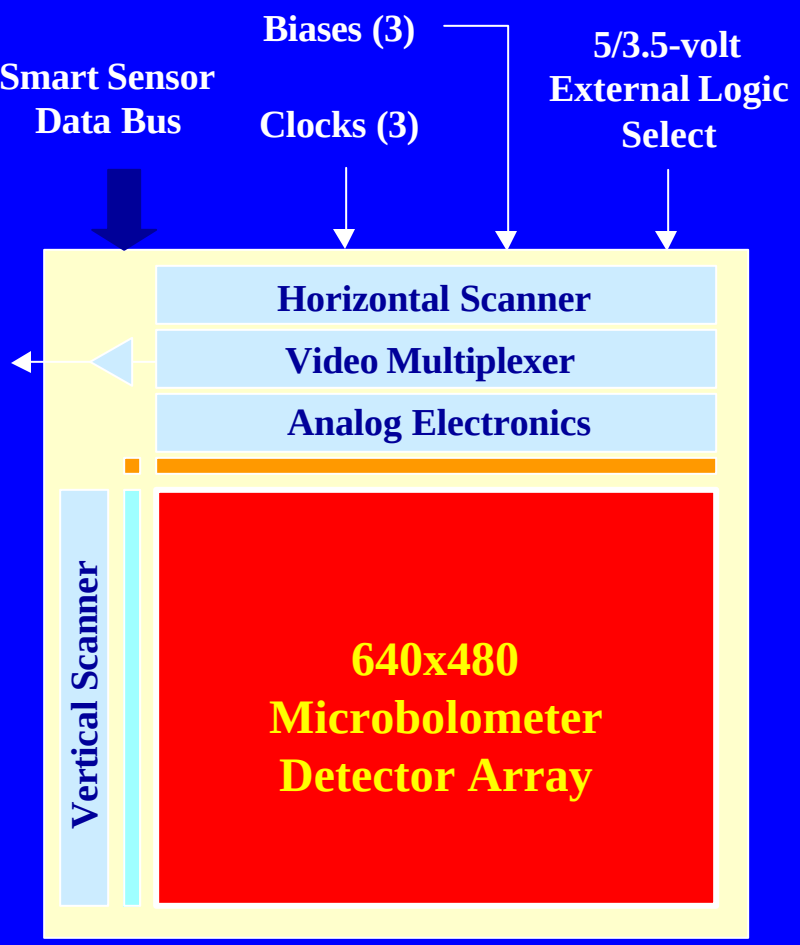
- **Higher resolution**
  - **More pixels in the focal plane without increasing die size**
  - **Pixel size reduction increases resolution with the same optics used for the U3000/U4000**
- **Smaller optics**
  - **The same resolution and FOV with smaller pixel size for the same array size (e.g. 320x240)**
  - **Lower optics and UFPA die cost**
- **Design Challenge – Smaller pixel size with no significant loss in thermal response sensitivity**

U6000 640x480 Product Objectives

- 25.4-micron pixel size (1-mil) with no significant loss in thermal response sensitivity
- Single channel 30-Hz video output, with externally selectable 2:1 interlaced or non interlaced full-frame video formats
- Incorporate, extend and improve “Smart-Sensor” features
  - Signal gain select – improved gain step uniformity
  - Detector bias selection and regulation – Improved stability versus temperature
  - Interlaced/Non-Interlaced video format selection
  - 6-bit resolution pixel offset compensation
  - Signal integration time and global video offset selection
- On-chip temperature measurement function (TEMP)
- Selectable 5-volt/3.5-volt external logic – Lower sensor power
- External bias supply requirements never exceed ± 5-volts

U6000 Design Architecture





Microbolometer Bridge

- Differential Output Suppresses...
  - Static & Dynamic Detector Bias
  - Detector Bias Supply Noise
- First Order UFPA Operating Temperature Drift Compensation

U6000 On-Chip Capabilities -1

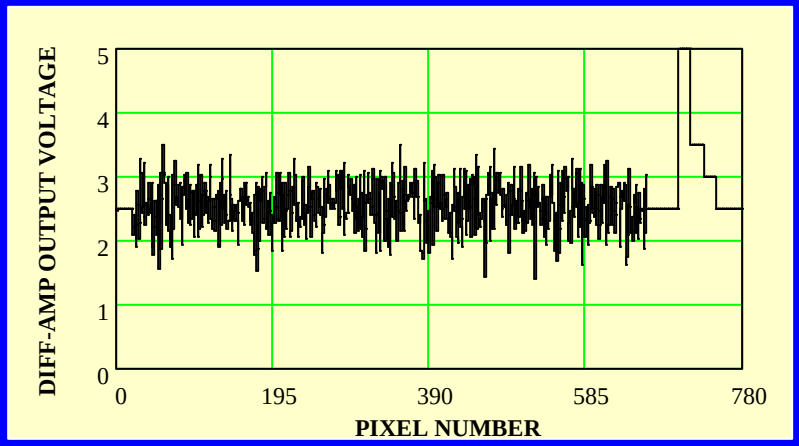
ON-CHIP CAPABILITY	DESCRIPTION OF CAPABILITY	CONTROL METHOD
Detector Bias Regulation (VDET)	On-chip detector bias selection that provides regulation better than a one part in 10^4, given a 1% external +5-volt bias supply	Externally generated 6-bit VDET data word on the Smart-Sensor bus
Signal Gain Selection (GAIN)	On-chip signal gain selection over > 6:1 range that enables more nearly constant responsivity for different optics and IR scenes. U6000 GAIN steps are more uniform.	Externally generated 3-bit GAIN data word on the Smart-Sensor bus
Signal Integration Time (INTEGRATION)	On-chip signal integration time selection from 0.0 μsec to ~ 52 μsec, which is used at DRS for diagnostics and performance tweaking.	Externally generated 3-bit INTEGRATION data word on the Smart-Senor bus
Pixel Offset compensation Coefficients (DAC)	On-chip offset compensation coefficients provided through the Smart-Bus to each pixel. Reduces level of pixel output offset variation from the detector pixels by a factor of ~ 63:1	Externally generated 6-bit DAC data words on the Smart-Sensor bus for each pixel.
Pixel Offset DAC Range (RANGE)	On-chip pixel offset compensation DAC LSB size selection covering an ~ 4:1 range. Used to select 'best' pixel offset correction sensitivity for each focal plane.	Externally generated 2-bit RANGE data word on the Smart-Sensor bus

U6000 On-Chip Capabilities -2

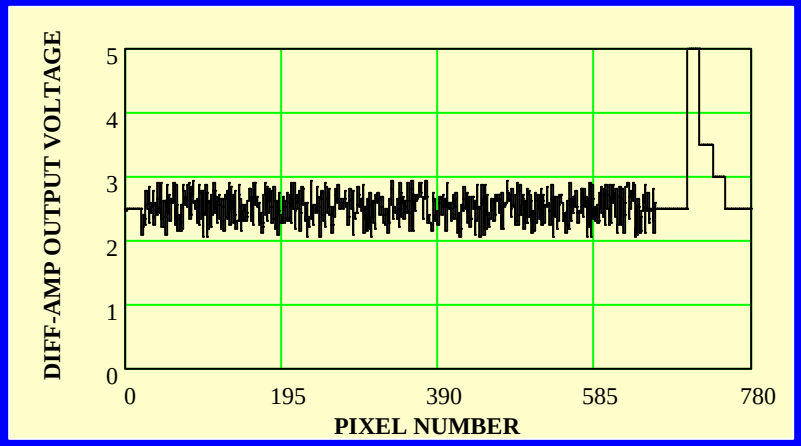
ON-CHIP CAPABILITY	DESCRIPTION OF CAPABILITY	CONTROL METHOD
Input Referred Voltage Offset (VOS)	On-chip selection of a global input referred detector voltage offset for the focal plane that can be used to compensate for large offsets.	Externally generated 7-bit VOS data word on Smart-Sensor bus.
Blind Reference Pixel Selection 1-8 (REFSEL 1-8)	External selection of any combination of up to eight Blind Reference bolometers for any row of the FPA, which can be used to improve operability and row offset uniformity.	Externally generated 1-bit RPSEL 1-8 command words on Smart-Sensor bus..
Interlace Selection (INTERLACE)	On-chip selection of either Interlaced or Non-Interlaced output video. The focal plane provides an odd/even field logic state during horizontal blanking.	Externally generated 3-bit INTERLACE command word on Smart-Sensor bus.
On-Chip Temperature Monitor (TEMP)	Six separate TEMP outputs (-30 to +60^{o}C) are streamed onto the output video line during horizontal blanking. Each output appears for 32 consecutive line times so that sample averaging can be used to improve resolution.	
5-volt/3.5-volt External Logic Selection	Allows the use of either 5-volt or > 3.3-volt external logic for lower sensor power.	Package pin-22 (0,+5-volts) = (+5,+3.5-volts)

U6000 Pixel Offset Correction

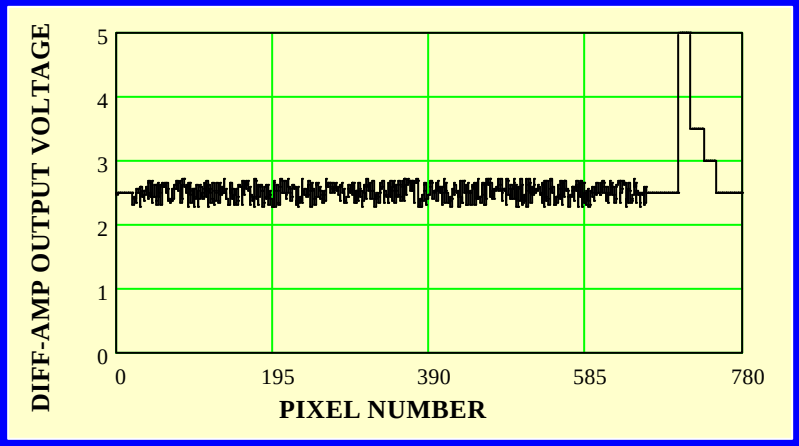
BEFORE PIXEL OFFSET CORRECTION



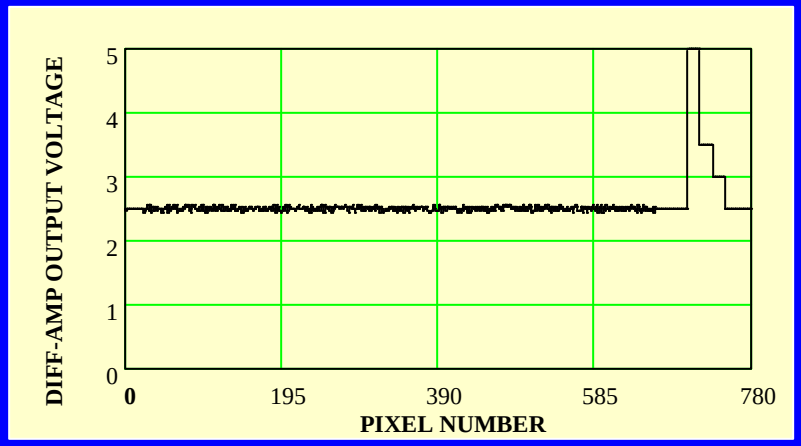
3-BIT PIXEL OFFSET CORRECTION



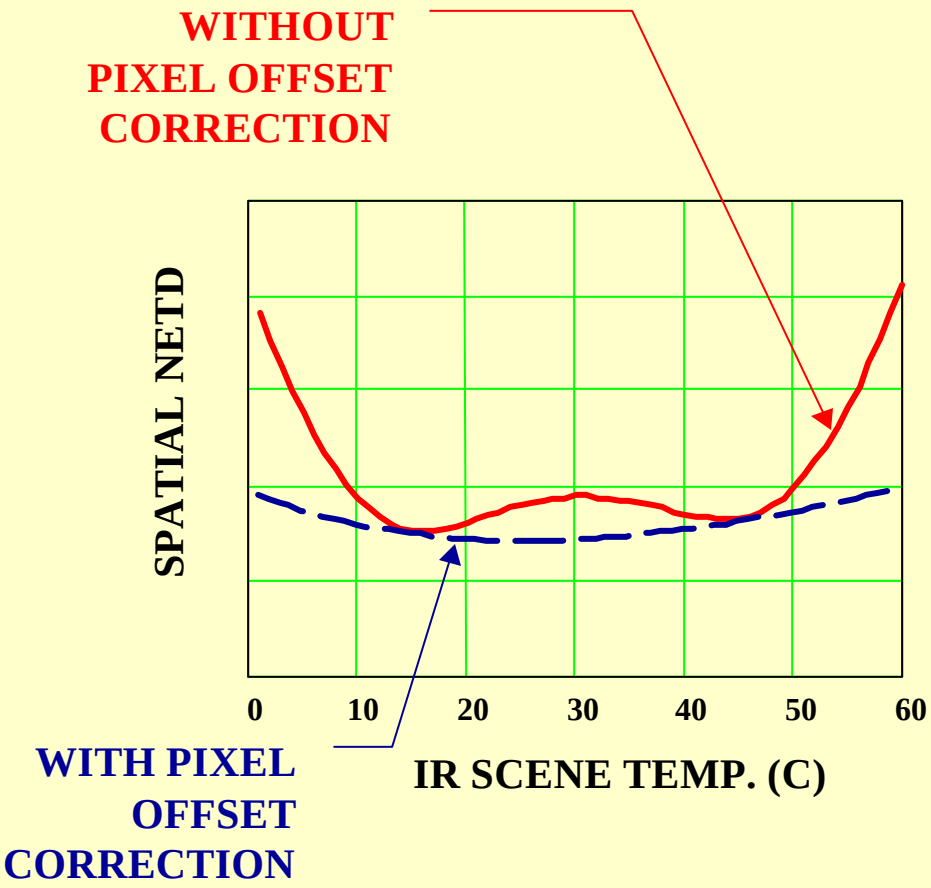
4-BIT PIXEL OFFSET CORRECTION



6-BIT PIXEL OFFSET CORRECTION



Spatial Noise Improved by Pixel Offset Correction



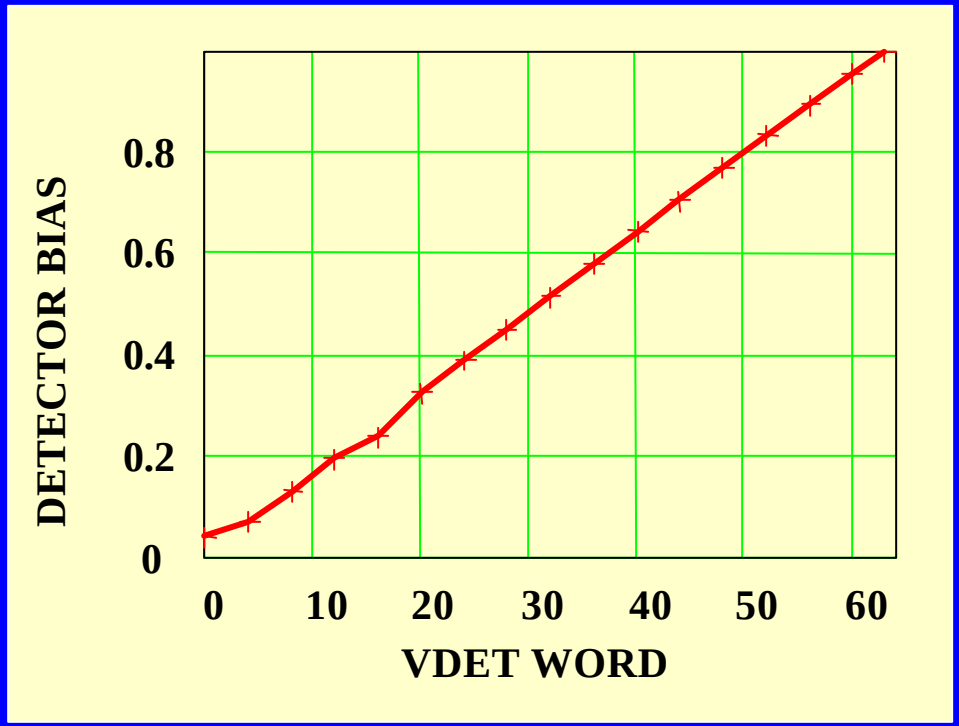
- Increased range of selectable on on-chip signal gains
  - Output video voltage range can be kept matched to sensor ADC for different optic speeds
- Significant reduction in the level of spatial offset pattern noise
  - Cleaner images over larger scene temperature calibration ranges

Validation of On-Chip Detector Bias Selection

- Demonstrated externally selectable detector bias capability in 64 uniform steps
- Bias regulation designed to achieve better than 100:1 external bias supply drift rejection
  - Overall bias regulation ~ 10,000:1 with 1% external +5-volt supply
  - Improves FPA stability as a function of operating temperature

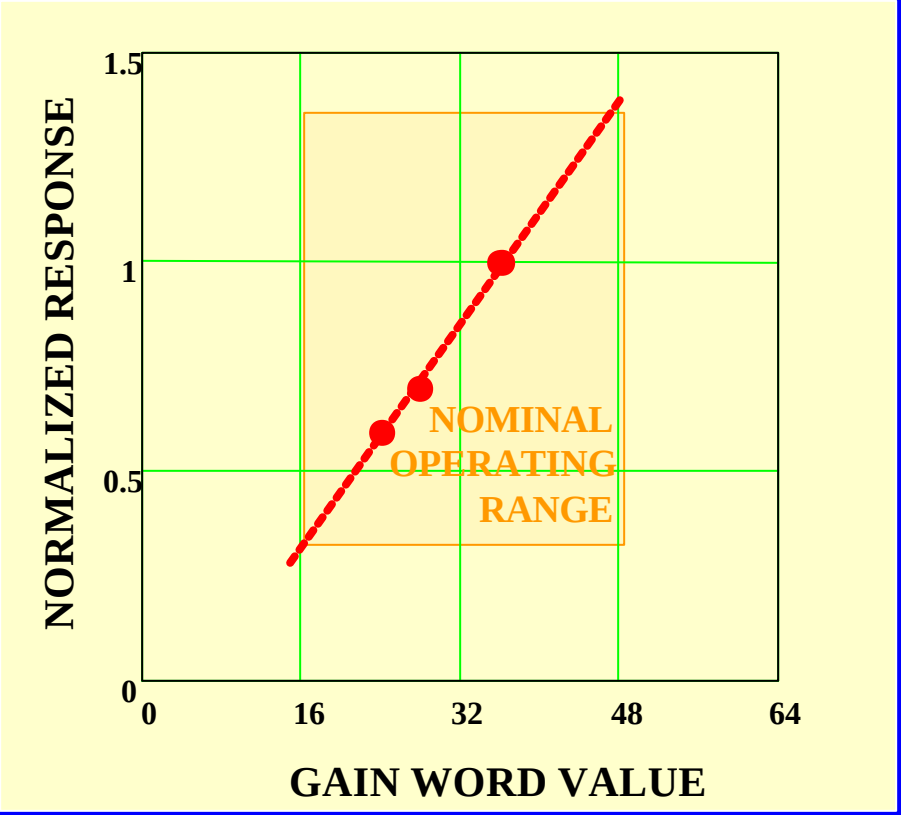
DETECTOR BIAS

(Normalized to maximum detector bias)



Response Versus Detector Bias

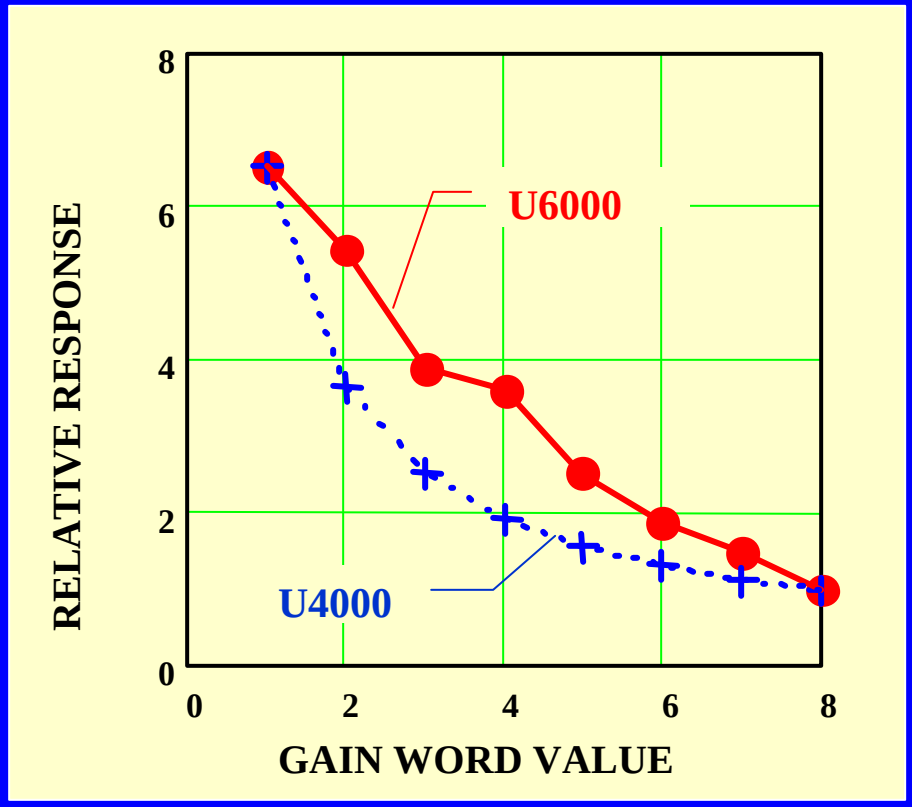
NORMALIZED THERMAL RESPONSE



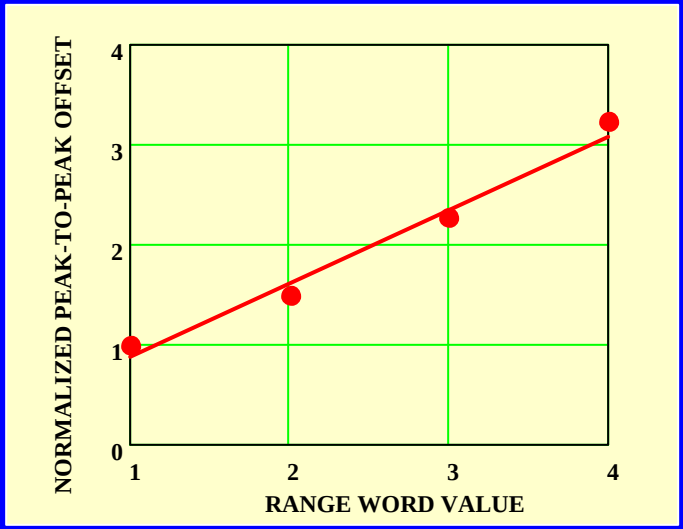
- **Demonstrated UFPA thermal response proportional to detector bias within nominal bias operating range**

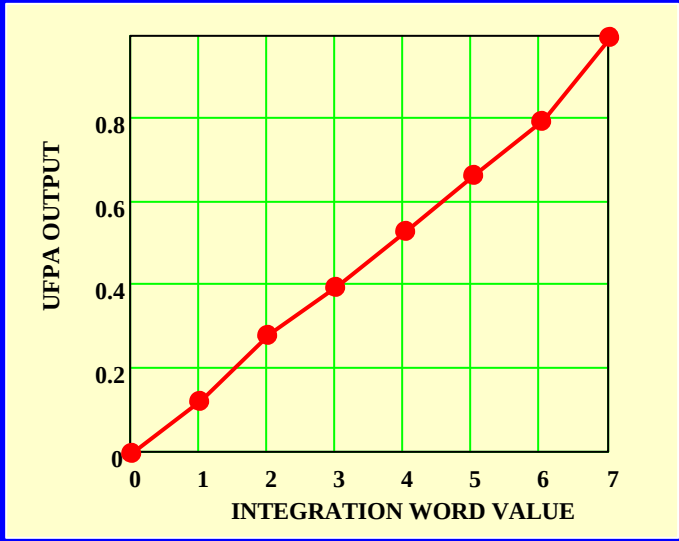
Validation of On-Chip Signal Gain Selection

- Demonstrated externally selectable gain range > 6:1
- Achieved improved uniformity between gain steps
  - Allows improved matching between video output range and sensor ADC input voltage range



RANGE and Integration Time Validation





- Validated RANGE function
  - Controls pixel offset correction DAC LSB size
  - Minimum LSB size used for U6000 Lot-1
- Validated INTEGRATION function
  - Controls signal integration time
  - Signal proportional to signal integration time

"First-Light" U6000 Video Demonstration

- **November 2001 – First U6000 wafer completed UFPA wafer processing at DRS**
- **December 2001**
  - **First U6000 wafer completed wafer functional probe testing, and die selected for vacuum packaging**
  - **First packaged U6000 die tested**
- **January 2002 – "First-Light"**
  - **U6000 integrated in general purpose IRFPA test camera**
  - **First U6000 imaging**
- **February 2002 – Video demonstration**
  - **Measured thermal response closely matches design predictions**
  - **Optimization of UFPA/sensor interface underway**

Summary

- DRS has demonstrated the U6000 640x480 UFPA
  - Functional validation completed
  - "First-Light" imaging demonstrated
- DRS pixel design innovation expected to increase U6000 thermal response sensitivity this year by another 30 to 40%
  - Improved pixel design completed, and UFPA wafer fabrication underway
  - Demonstration planned for early this fall
- 25.4-micron pixel size 320x240 UFPA design (U7000)
  - Identical design architecture, performance and electrical interface as U6000
  - Will allow optics to be down-sized, and has significant producibility advantages relative to 51-micron pixel size 320x240 UFPA products